In the Claims:

Please amend the claims as indicated below.

1. (Canceled)

2. (Previously Presented) The integrated circuit of claim 11, wherein the test response analysis unit comprises a multiple input shift register to compress the test response vectors into a checksum that can be checked against a reference.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The ~~tester~~ arrangement of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic ~~and~~ logic unit and ~~generates~~ the programmable test vector generator is programmed to generate test vectors in real time.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Currently Amended) A circuit arrangement comprising:

a tester ~~for testing logic circuitry of an integrated circuit, comprising~~ that includes a programmable test vector generator for generating test vectors ~~for the logic circuitry;~~ and

an integrated circuit that includes

logic circuitry to be tested using the test vectors,

a test control block to control testing of the logic circuitry, and

a test response and analysis unit configured and arranged to receive test results from the logic circuitry in response to the test vectors, to produce a compact representation of said test results, and to output said compact representation to the tester.

11. (Previously Presented) An integrated circuit comprising:

logic circuitry to be tested using test vectors generated by an external tester;

a test control block to control testing of the logic circuitry; and

a test response and analysis unit to receive test results from the logic circuitry in response to the test vectors, to produce a compact representation of said test results, and to output said compact representation to the external tester.

12. (Currently Amended) A method of testing logic circuitry of an integrated circuit, the integrated circuit including a test response analysis unit, the method comprising:

generating within an external tester test vectors for testing the logic circuitry, using a programmable test vector generator; ~~and~~

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry;

the test response analysis unit receiving from the logic circuitry test results in response to the test vectors and producing a compact representation of said test results; and

outputting said compact representation to the external tester.

13. (Canceled)

14. (Currently Amended) The method of claim 12 [[13]] wherein said compact presentation includes test vectors applied directly to the external tester to enable fault localization on the logic circuitry.

15. (Currently Amended) The ~~tester~~ arrangement of claim 10, wherein the programmable test vector generator is programmed to generate pseudo-random test vectors and deterministic test vectors for the logic circuitry.

16. (Currently Amended) The ~~tester~~ arrangement of claim 10, wherein the programmable test vector generator is programmed to generate test vectors for the logic circuitry in real time.

17. (Previously Presented) The method of claim 12, further comprising programming the programmable test vector generator to modify the test vectors based on the logic circuitry to be tested.

18. (Previously Presented) The method of claim 12, further comprising programming the programmable test vector generator to generate test vectors for the logic circuitry in real time.

19. (Previously Presented) The method of claim 12, further comprising programming the programmable test vector generator to generate test pseudo-random test vectors and deterministic test vectors for the logic circuitry.